

Homework 10

Due: Saturday 2/21 at 11:59pm

Complete the following problems, which should be submitted on paper or via email.

1. (6 points) In this problem, you will create sequences of address requests for 4-line fully-associative caches. For convenience, I suggest that you name your cache lines “A”, “B”, etc.
 - (a) Give a sequence of accesses such that a LRU replacement policy incurs fewer cache misses than a FIFO replacement policy.
 - (b) Give a sequence of accesses such that a FIFO replacement policy incurs fewer cache misses than a LRU replacement policy.
2. (10 points) Consider a 4-line cache direct-mapped write-back cache, where each line contains two words. Give the tag, valid bit, and dirty bit associated with each cache line after each operation in the sequence below. Note that the addresses are given in binary and include ALL bits of the address, even the two least significant bits used to address within a word.
 - lw 1000000
 - sw 1110100
 - lw 1000100
 - sb 1101010
 - lw 1110000
 - sb 1110111
 - lbu 0100001
 - lw 0111100
 - sw 0111100
 - lbu 0110010